

## AD8691/AD8692/AD8694

### FEATURES

- Offset voltage: 400  $\mu$ V typical**
- Low offset voltage drift: 6  $\mu$ V/ $^{\circ}$ C maximum  
(AD8692/AD8694)**
- Very low input bias currents: 1 pA maximum**
- Low noise: 8 nV/ $\sqrt{\text{Hz}}$**
- Low distortion: 0.0006%**
- Wide bandwidth: 10 MHz**
- Unity-gain stable**
- Single-supply operation: 2.7 V to 6 V**

### APPLICATIONS

- Photodiode amplification**
- Battery-powered instrumentation**
- Medical instruments**
- Multipole filters**
- Sensors**
- Portable audio devices**

### GENERAL DESCRIPTION

The AD8691, AD8692, and AD8694 are low cost, single, dual, and quad rail-to-rail output, single-supply amplifiers featuring low offset and input voltages, low current noise, and wide signal bandwidth. The combination of low offset, low noise, very low input bias currents, and high speed make these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from this combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion of these devices.

Applications for these amplifiers include power amplifier (PA) controls, laser diode control loops, portable and loop-powered instrumentation, audio amplification for portable devices, and ASIC input and output amplifiers.

The small SC70 and TSOT package options for the AD8691 allow it to be placed next to sensors, thereby reducing external noise pickup.

The AD8691, AD8692, and AD8694 are specified over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The AD8691 single is available in 5-lead SC70 and 5-lead TSOT packages. The AD8692 dual is available in 8-lead MSOP and narrow SOIC surface-mount packages. The AD8694 quad is available in 14-lead TSSOP and narrow 14-lead SOIC packages.

### PIN CONFIGURATIONS

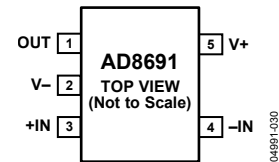


Figure 1. 5-Lead TSOT

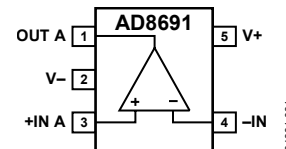


Figure 2. 5-Lead SC70



Figure 3. 8-Lead MSOP

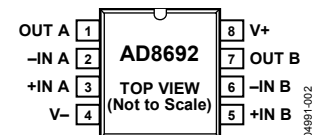


Figure 4. 8-Lead SOIC

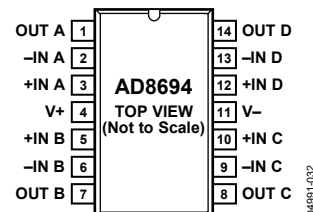


Figure 5. 14-Lead SOIC

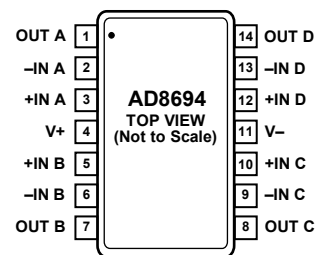


Figure 6. 14-Lead TSSOP

### Rev. C

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**REVISION HISTORY**

**5/07—Rev. B to Rev. C**

Change to Figure 1 .....	1
Changes to Large Signal Voltage Gain Values in Table 1 .....	3
Change to Phase Margin Symbol in Table 1 .....	3
Change to TA Value for Table 2 .....	4
Changes to Large Signal Voltage Gain Values in Table 2 .....	4
Change to Phase Margin Symbol in Table 2 .....	4
Changes to Table 4.....	5
Changes to Outline Dimensions.....	11
Changes to Ordering Guide .....	12

**3/05—Rev. A to Rev. B**

Added AD8694 .....	Universal
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**1/05—Rev. 0 to Rev. A**

Added AD8691 .....	Universal
Changes to Features.....	1
Added Figure 1 and Figure 2.....	1
Changes to Electrical Characteristics .....	3
Changes to Figure 6 caption.....	6
Changes to Figure 9.....	6
Updated Outline Dimensions .....	11
Changes to Ordering Guide .....	11

**10/04—Revision 0: Initial Version**

## ELECTRICAL CHARACTERISTICS

$V_S = 2.7\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = -0.3\text{ V to }+1.6\text{ V}$ $V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.4	2.0	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range			-0.3		+1.6	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.3\text{ V to }+1.6\text{ V}$ $V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$	68	90		dB
Large Signal Voltage Gain	$A_{VO}$		60	85		dB
AD8691/AD8692		$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to }2.2\text{ V}$	90	250		V/mV
AD8694		$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to }2.2\text{ V}$	60			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					
AD8691				2	12	$\mu\text{V}/^\circ\text{C}$
AD8692/AD8694				1.3	6	$\mu\text{V}/^\circ\text{C}$
<b>INPUT CAPACITANCE</b>						
Common-Mode Input Capacitance	$C_{CM}$			5		pF
Differential Input Capacitance	$C_{DM}$			2.5		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.64	2.66		V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.6			V
Short-Circuit Current	$I_{SC}$			25	40	mV
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$			60	mV
				$\pm 20$		mA
				12		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80	95		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	75	95		dB
				0.85	0.95	mA
					1.2	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		5		V/ $\mu\text{s}$
Settling Time	$t_S$	To 0.01%		1		$\mu\text{s}$
Gain Bandwidth Product	GBP			10		MHz
Phase Margin	$\phi_m$			60		Degrees
Total Harmonic Distortion + Noise	THD + N	$G = 1$ , $R_L = 600\ \Omega$ , $f = 1\text{ kHz}$ , $V_O = 250\text{ mV p-p}$		0.003		%
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		1.6	3.0	$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		8	12	nV/ $\sqrt{\text{Hz}}$
	$e_n$	$f = 10\text{ kHz}$		6.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		pA/ $\sqrt{\text{Hz}}$

# AD8691/AD8692/AD8694

$V_S = 5.0\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = -0.3\text{ V to }+3.9\text{ V}$ $V_{CM} = -0.1\text{ V to }+3.9\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.4	2.0	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range			-0.3		+3.9	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.3\text{ V to }+3.9\text{ V}$ $V_{CM} = -0.1\text{ V to }+3.9\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$	70	95		dB
Large Signal Voltage Gain	$A_{VO}$	$V_O = 0.5\text{ V to }4.5\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_{CM} = 0\text{ V}$ $V_O = 0.5\text{ V to }4.5\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_{CM} = 0\text{ V}$	250	2000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					$\mu\text{V}/^\circ\text{C}$
AD8691				2	12	$\mu\text{V}/^\circ\text{C}$
AD8692/AD8694				1.3	6	$\mu\text{V}/^\circ\text{C}$
<b>INPUT CAPACITANCE</b>						
Common-Mode Input Capacitance	$C_{CM}$			5		pF
Differential Input Capacitance	$C_{DM}$			2.5		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C to }+125^\circ\text{C}$	4.96	4.98		V
			4.7	4.78		V
			4.6			V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C to }+125^\circ\text{C}$ $-40^\circ\text{C to }+125^\circ\text{C}$		20	40	mV
AD8691/AD8692				165	210	mV
AD8694				185	240	mV
AD8691/AD8692					290	mV
AD8694					370	mV
Short-Circuit Current	$I_{SC}$			$\pm 80$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		10		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80	95		dB
			75	95		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.95	1.05	mA
					1.3	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		5		V/ $\mu\text{s}$
Settling Time	$t_S$	To 0.01%		1		$\mu\text{s}$
Full Power Bandwidth	$BW_P$	<1% distortion		360		kHz
Gain Bandwidth Product	GBP			10		MHz
Phase Margin	$\phi_m$			65		Degrees
Total Harmonic Distortion + Noise	THD + N	$G = 1$ , $R_L = 600\ \Omega$ , $f = 1\text{ kHz}$ , $V_O = 1\text{ V p-p}$		0.0006		%
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		1.6	3.0	$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		8	12	nV/ $\sqrt{\text{Hz}}$
	$e_n$	$f = 10\text{ kHz}$		6.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		pA/ $\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Differential Input Voltage	$\pm 6\text{ V}$
Output Short-Circuit Duration to GND	Observe derating curves
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Operating Temperature Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Junction Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

$\theta_{JA}$  is specified for the worst-case conditions, that is, the device soldered in the circuit board for surface-mount packages.

**Table 4. Thermal Resistance**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead MSOP (RM-8)	210	45	$^\circ\text{C}/\text{W}$
8-Lead SOIC (R-8)	158	43	$^\circ\text{C}/\text{W}$
5-Lead TSOT (UJ-5)	207	61	$^\circ\text{C}/\text{W}$
5-Lead SC70 (KS-5)	376	126	$^\circ\text{C}/\text{W}$
14-Lead TSSOP (RU-14)	180	35	$^\circ\text{C}/\text{W}$
14-Lead SOIC (R-14)	120	36	$^\circ\text{C}/\text{W}$

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = +5\text{ V}$  or  $\pm 2.5\text{ V}$ , unless otherwise noted.

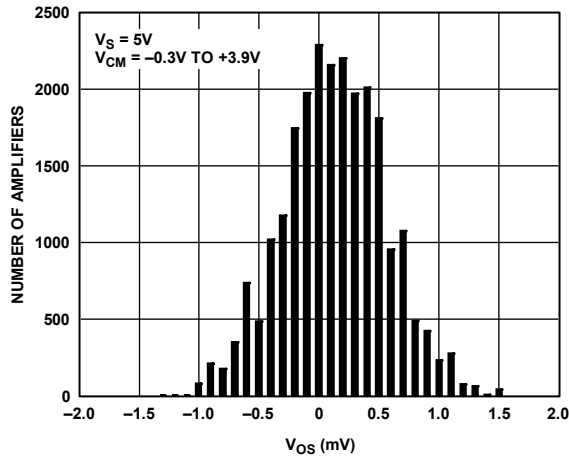


Figure 7. Input Offset Voltage Distribution

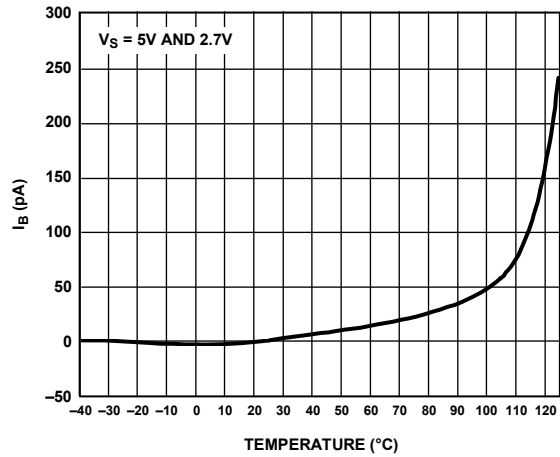


Figure 10. Input Bias Current vs. Temperature

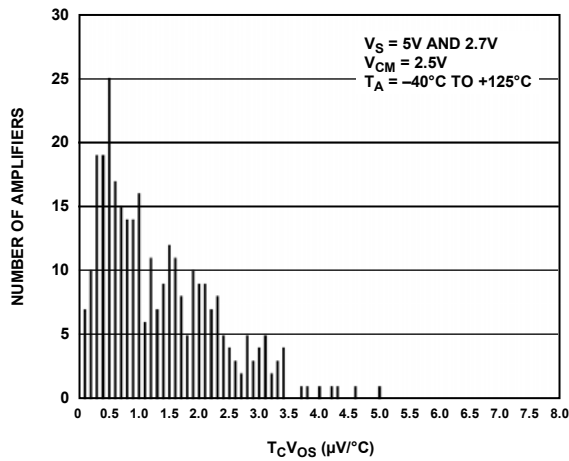


Figure 8. AD8692/AD8694 Input Offset Voltage Drift Distribution

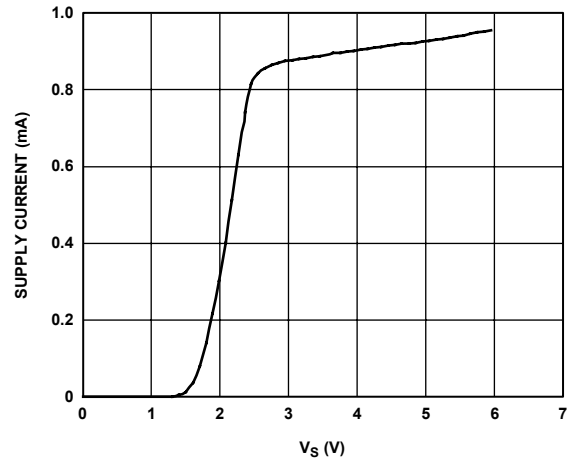


Figure 11. Supply Current vs. Supply Voltage

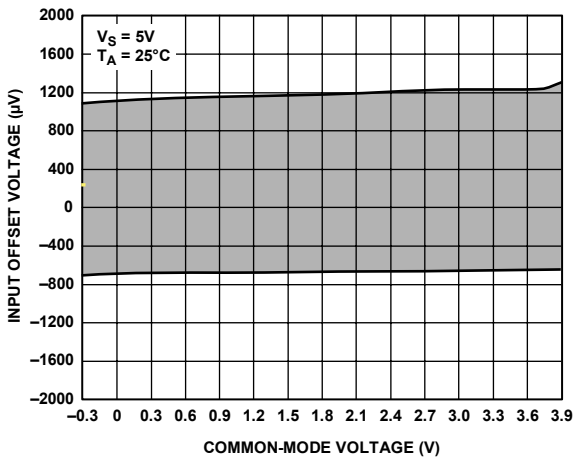


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

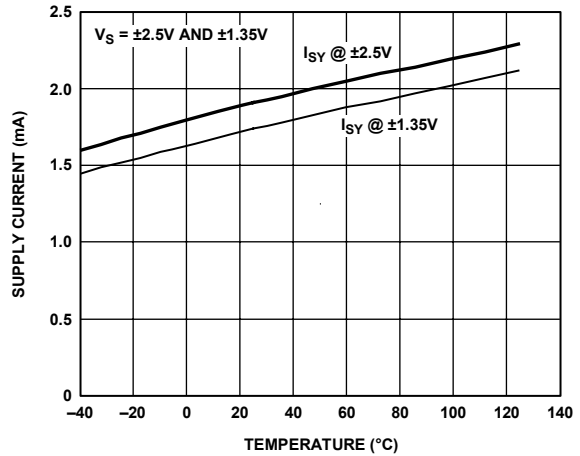


Figure 12. Supply Current vs. Temperature

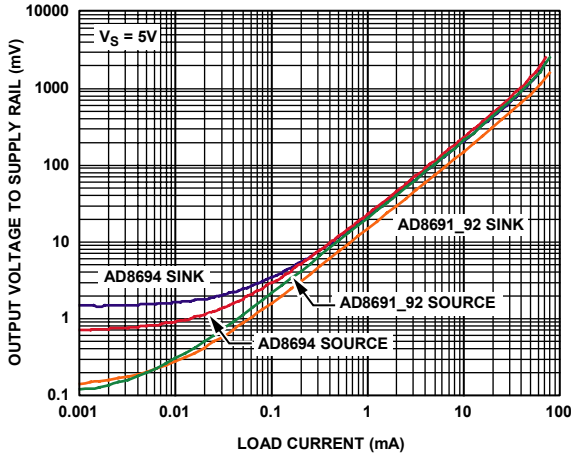


Figure 13. Output Voltage to Supply Rail vs. Load Current

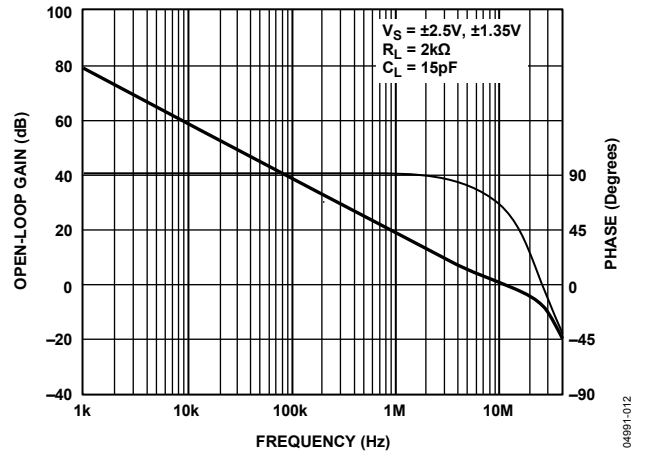


Figure 16. Open-Loop Gain and Phase vs. Frequency

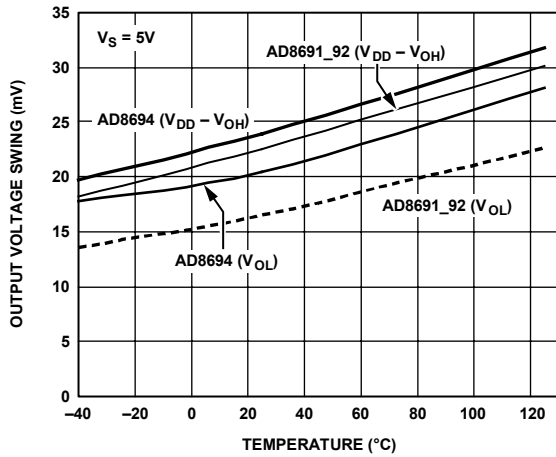


Figure 14. Output Voltage Swing vs. Temperature ( $I_L = 1 \text{ mA}$ )

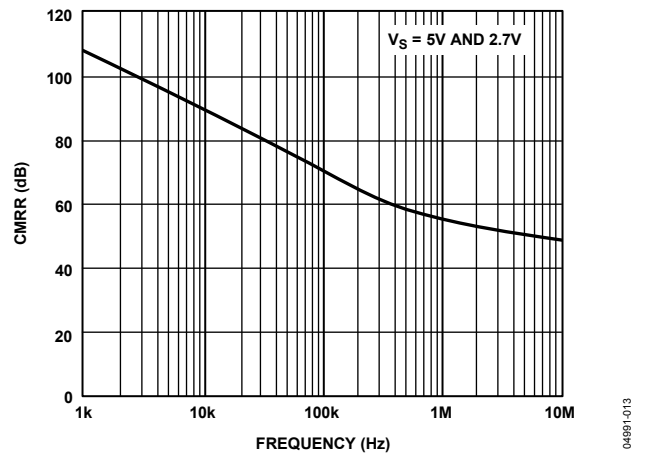


Figure 17. CMRR vs. Frequency

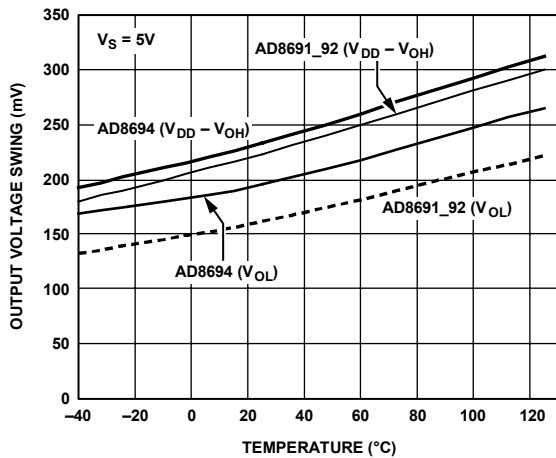


Figure 15. Output Voltage Swing vs. Temperature ( $I_L = 10 \text{ mA}$ )

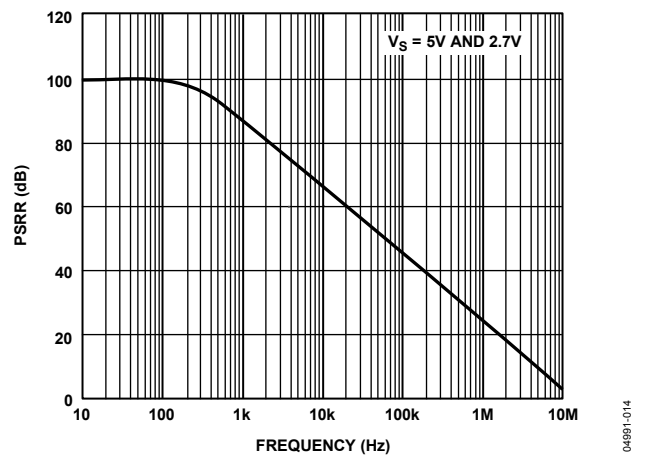


Figure 18. PSRR vs. Frequency

# AD8691/AD8692/AD8694

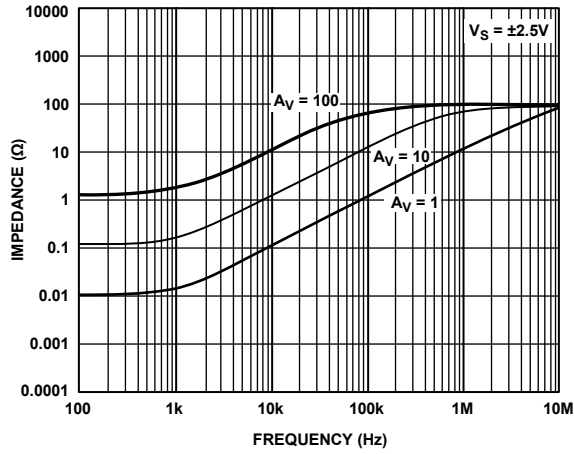


Figure 19. Closed-Loop Output Impedance vs. Frequency

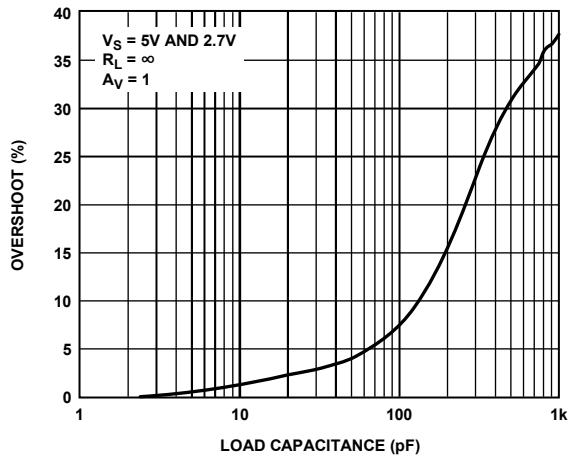


Figure 20. Small Signal Overshoot vs. Load Capacitance

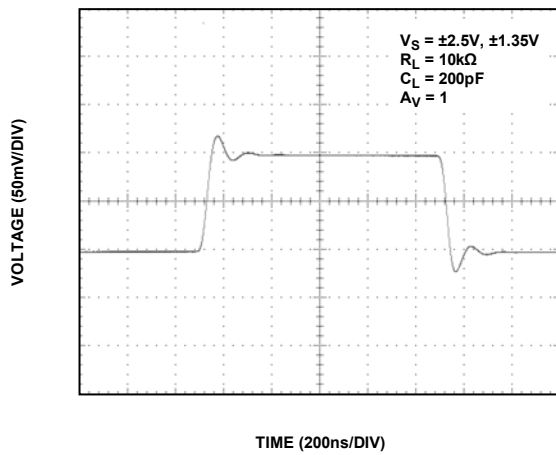


Figure 21. Small Signal Transient Response



Figure 22. Large Signal Transient Response



Figure 23. Positive Overload Recovery



Figure 24. Negative Overload Recovery

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04991-016

04991-017

04991-018

04991-019

04991-020



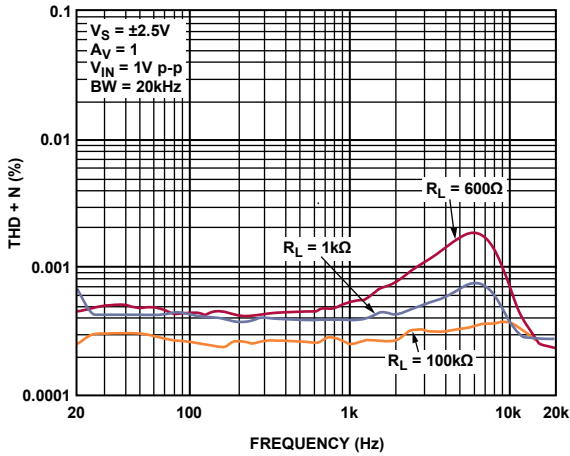


Figure 25. THD + N vs. Frequency

04891-021

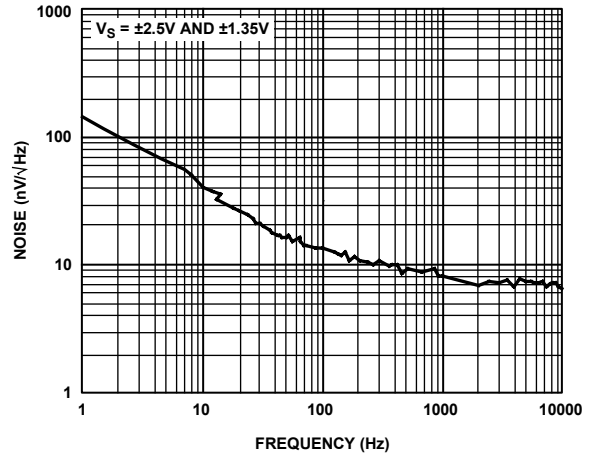


Figure 27. Voltage Noise Density

04891-023



Figure 26. 0.1 Hz to 10 Hz Input Voltage Noise

04891-022

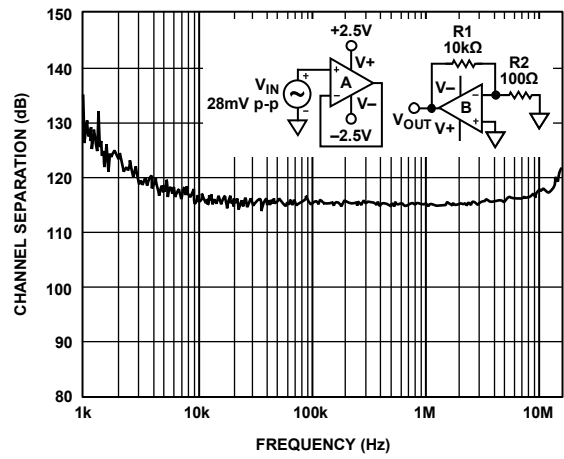


Figure 28. AD8692/AD8694 Channel Separation

04891-024

# AD8691/AD8692/AD8694

$V_S = +2.7\text{ V}$  or  $\pm 1.35\text{ V}$ , unless otherwise noted.

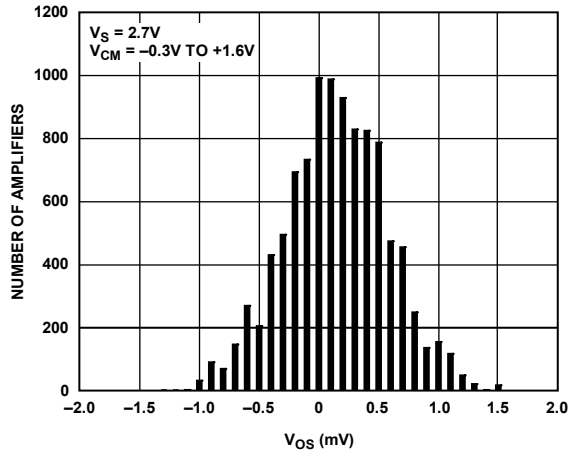


Figure 29. Input Offset Voltage Distribution

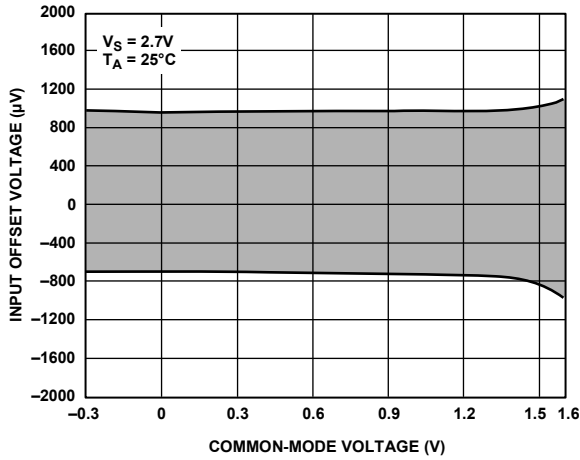


Figure 30. Input Offset Voltage vs. Common-Mode Voltage

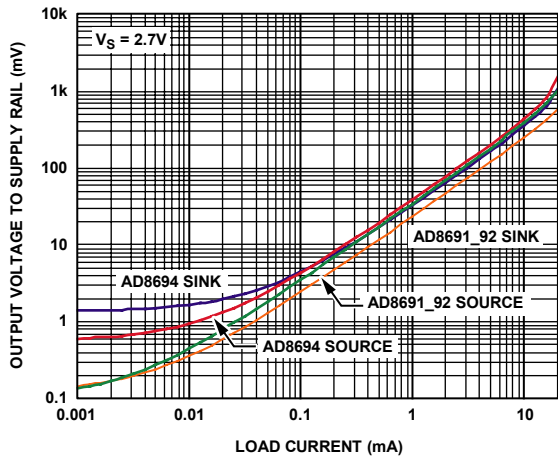


Figure 31. Output Voltage to Supply Rail vs. Load Current

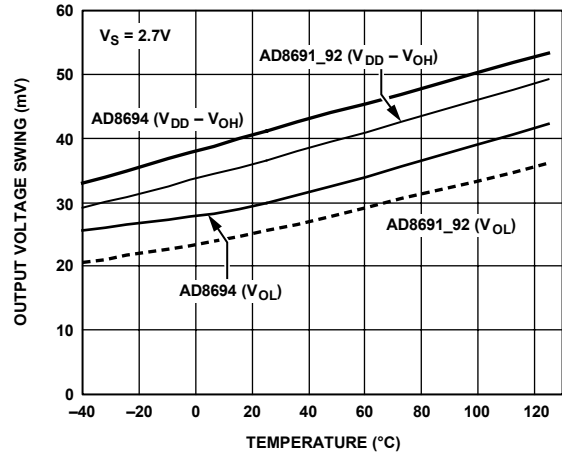


Figure 32. Output Voltage Swing vs. Temperature ( $I_L = 1\text{ mA}$ )



Figure 33. Large Signal Transient Response

04991-025

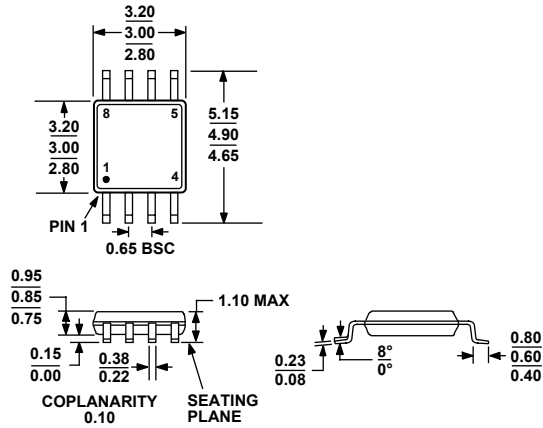
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04991-026

04991-029

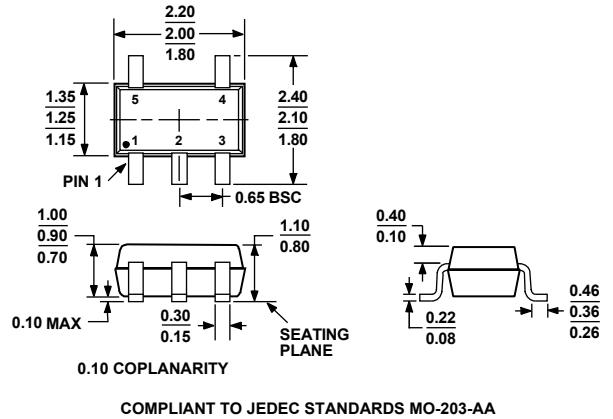
04991-027

# OUTLINE DIMENSIONS



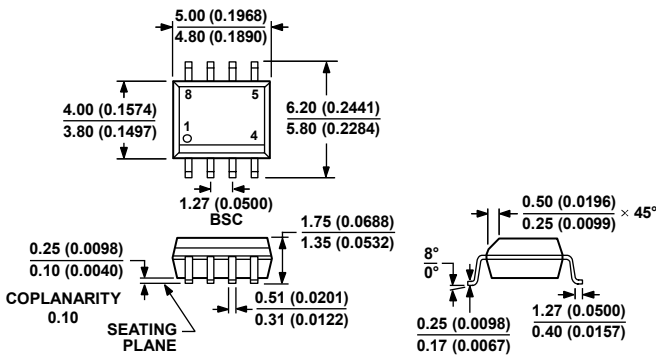
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 34. 8-Lead Mini Small Outline Package [MSOP] (RM-8)  
Dimensions shown in millimeters



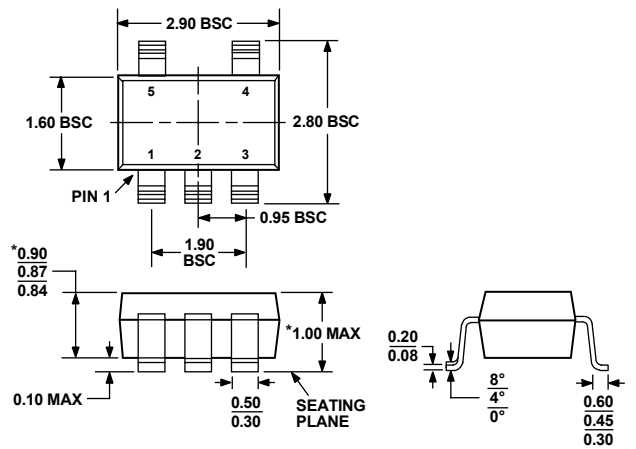
COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 36. 5-Lead Thin Shrink Small Outline Package [SC70] (KS-5)  
Dimensions shown in millimeters



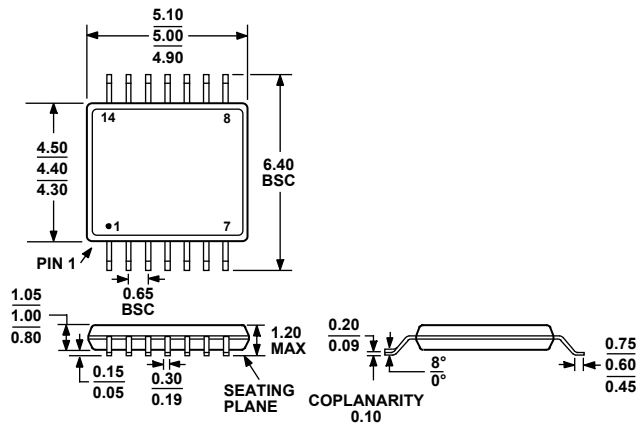
COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)  
Dimensions shown in millimeters and (inches)



\*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

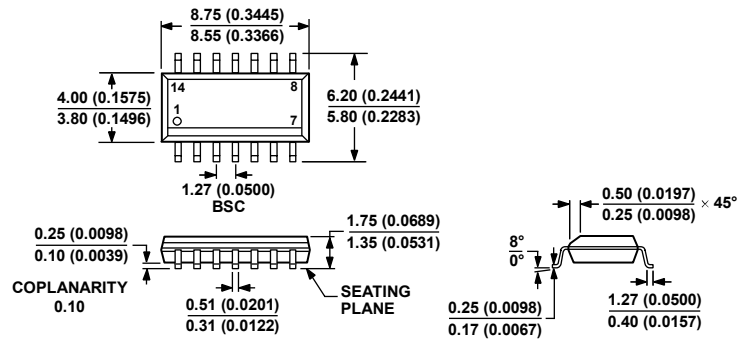
Figure 37. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)  
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 38. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)  
Dimensions shown in millimeters

# AD8691/AD8692/AD8694



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 39. 14-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body (R-14)  
 Dimensions shown in millimeters

0160606-A

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8691AUJZ-R2 <sup>1</sup>	-40°C to +125°C	5-Lead TSOT	UJ-5	ACA
AD8691AUJZ-REEL <sup>1</sup>	-40°C to +125°C	5-Lead TSOT	UJ-5	ACA
AD8691AUJZ-REEL7 <sup>1</sup>	-40°C to +125°C	5-Lead TSOT	UJ-5	ACA
AD8691AKSZ-R2 <sup>1</sup>	-40°C to +125°C	5-Lead SC70	KS-5	ACA
AD8691AKSZ-REEL <sup>1</sup>	-40°C to +125°C	5-Lead SC70	KS-5	ACA
AD8691AKSZ-REEL7 <sup>1</sup>	-40°C to +125°C	5-Lead SC70	KS-5	ACA
AD8692ARMZ-R2 <sup>1</sup>	-40°C to +125°C	8-Lead MSOP	RM-8	APA
AD8692ARMZ-REEL <sup>1</sup>	-40°C to +125°C	8-Lead MSOP	RM-8	APA
AD8692ARZ <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8692ARZ-REEL <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8692ARZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8694ARUZ <sup>1</sup>	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8694ARUZ-REEL <sup>1</sup>	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8694ARZ <sup>1</sup>	-40°C to +125°C	14-Lead SOIC_N	R-14	
AD8694ARZ-REEL <sup>1</sup>	-40°C to +125°C	14-Lead SOIC_N	R-14	
AD8694ARZ-REEL7 <sup>1</sup>	-40°C to +125°C	14-Lead SOIC_N	R-14	

<sup>1</sup> Z = RoHS Compliant Part.